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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,376	09/15/2004	Cheng-Hsiung Chen	NAUP0525USA	5375

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EXAMINER	
FULK, STEVEN J	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,376	CHEN, CHENG-HSIUNG	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   a. Claim 1 is vague and indefinite in the describing the position of the dielectric layer and polysilicon layer relative to the substrate. Claim 1 first recites "a substrate comprising a dielectric layer," but then alternatively recites "removing...the dielectric layer...down to the surface of the substrate." It is not reasonably clear whether the dielectric layer is (1) a part of the substrate or (2) separate from and on the substrate.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Bourassa '378. Bourassa discloses the method of forming a high resistance region of a polysilicon resistor comprising providing a substrate, the substrate comprising a dielectric layer, forming a polysilicon layer on the dielectric layer, and doping the polysilicon layer to form a low resistance region and a high resistance region, where N-type and P-type dopants having the same order of magnitude are used to form the high resistance region (column 3, lines 22-42 and column 4, line 66 – column 5, line 13).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Insofar as definite, claims 1-6 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bourassa '378 in view of Kim '333.

a. Regarding claims 1-3, Bourassa teaches the elements as set forth immediately above, but the reference does not teach the method of removing portions of the polysilicon layer and dielectric layer to the

surface of the substrate. Kim shows the method of removing polysilicon and dielectric layers to the surface of the substrate (column 3, lines 28-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove portions of the polysilicon and dielectric layers down to the substrate because patterning semiconductor layers into discrete components was one of the limited number of conventional methods for forming semiconductor devices.

b. Regarding claims 1, 4, 6, 10, 11, and 13, Bourassa teaches the elements as set forth above, but the reference does not teach the method of forming a salicide block on portions of the polysilicon with high resistance and forming a salicide layer on portions of the polysilicon layer with low resistance on either side of the high resistance region. Kim shows the use of the salicide block over the high resistance region of the resistor to insulate it and a salicide layer at either end of the resistor to be used as electrical contacts (column 3, lines 53-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a salicide block to insulate resistor regions and to use a salicide layer to electrically connect resistor regions because the use of salicides

was a conventional method of further reducing polysilicon resistance using self-aligning metal layers.

c. Regarding claims 5 and 12, Bourassa teaches the elements as set forth above, but the reference does not teach the method of forming an inter layer dielectric on the substrate comprising a contact hole to the salicide layer and a conductive layer on portions of the inter layer dielectric and within the contact hole. Kim shows the use of an inter layer dielectric on the substrate, which is etched to form contact holes connecting to the salicide layer, and a metal layer deposited on portions of the dielectric and within the contact holes (column 3, line 60 - column 4, line 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an inter layer dielectric and conductive layer because layers of dielectric and conductive material enable interconnection between semiconductor devices and external components so that the devices can perform their intended function.

Response to Arguments

7. Applicant's arguments filed August 17, 2005 have been fully considered but they are not persuasive.

a. Regarding claims 7-9, the applicant argues that the polysilicon resistor of Bourassa will form a PN junction when the center resistor region of the polysilicon layer includes both type of dopants and the side regions of the polysilicon layer include only one type of dopant.

This argument is not persuasive because reference teaches doping the center resistor region with an n-type dopant and a p-type dopant of equal concentrations (col. 5, lines 5-7). Thus, no PN junction would be formed and the high resistance region of Bourassa would have the same structure as applicant's high resistance region, as claimed.

Also, the argument is not persuasive because the claims are written broadly enough to read on a resistor having two PN junctions when modified with salicide contacts.

b. Regarding claims 1-3, applicant argues that the combination of Kim and Bourassa never suggested the characteristics of the claimed invention. In fact, Bourassa teaches the use of two different types of dopants at the same time to adjust polysilicon resistance in the high resistance region of a polysilicon resistor, and Kim teaches the formation of a salicide layer to reduce the polysilicon resistance in the low resistance region of the polysilicon resistor.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references

individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

c. Regarding claims 1, 4, 6, 10, 11, and 13, the applicant argues that "Kim never teaches the means of utilizing the formation of a salicide layer via the low resistance region to reduce the polysilicon resistance in the low resistance region." The meaning of the applicant's argument is not clear. If the argument means that Kim does not teach the formation of a salicide layer improves conductivity, please note col. 1, lines 18-21 of Kim. If the argument means the reference does not teach how the formation of a salicide layer reduces resistance, the argument is not persuasive because there is no requirement for a prior art reference to expressly recite the underlying theory or physics by which a device functions.

d. Regarding claims 5 and 12, the applicant argues that the claims are allowable based on their dependency on claims 1 and 7. The arguments for the independent claims are addressed above.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf
8/24/05

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER